WE CLAIM:

1. An electronic circuit comprising:

a nonvolatile memory further comprising a p type semiconductor substrate, a first isolation layer over the p type semiconductor substrate, a trapping layer over the first isolation layer, a second isolation layer over the trapping layer, a gate over the second isolation layer, two N+ junctions in the p type semiconductor substrate, and a source and a drain respectively formed on the N+ junctions;

the trapping layer being operable to retain electrons in an erase state for at least one bit in the nonvolatile memory, causing the nonvolatile memory to have a threshold voltage, and a read current in a reading operation; and

a comparator receiving a first input resulting from the read current and a second input in a form of one of a reference voltage and a reference current.

2. The circuit of claim 1 wherein the threshold voltage of the at least one bit in an erase state is larger than the threshold voltage of the at least one bit in a program state..

3. The circuit of claim 1 wherein the read current caused by the at least one bit in an erase state is lower than the read current caused by the at least one bit in a program state.

4. The circuit of claim 1, the first isolation layer and the second isolation layer further comprising silicon oxide.

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5. The circuit of claim 1, the trapping layer further comprising nitride.

6. A system comprising:

a nonvolatile memory further comprising a p type semiconductor substrate, a first isolation layer over the p type semiconductor substrate, a trapping layer over the first oxide layer, a second isolation layer over the nitride layer, a gate over the second isolation layer, two N+ junctions in the p type semiconductor substrate, a source and a drain respectively formed on the N+ junctions;

the trapping layer being operable to retain electrons in an erase state for one of a drain bit and a source bit in the nonvolatile memory, causing the memory to have a threshold voltage, and a read current in a reading operation; and

a comparator receiving a first input resulting from the read current and a second input in a form of one of a reference voltage and a reference current.

7. The system of claim 6 wherein a bias voltage is applied to the source and the drain for reading the drain bit and the source bit, respectively.

8. The system of claim 6 wherein electric holes are injected at the drain and the source for programming the drain bit and the source bit, respectively.

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9. The system of claim 6 wherein the threshold voltage of one of the drain bit and the source bit in an erase state is larger than the threshold voltage of one of the drain bit and the source bit in a program state.

10. The system of claim 6 wherein the read current caused by one of the drain bit and the source bit in an erase state is lower than the read current caused by one of the drain bit and the source bit in a program state.

11. A system having a nonvolatile memory comprising:

a semiconductor substrate further comprising a source, a drain, and a channel formed between the source and drain when the nonvolatile memory is read;

a first isolating layer over the channel;

a nonconducting trapping layer over the first isolating layer;

a second isolating layer over the nonconducting trapping layer;

a gate over the second isolating layer; and

a first bit and a second bit in the nonvolatile memory;

wherein the nonconducting trapping layer retains electrons in an erase state for the nonvolatile memory.

12. The system of claim 11 further comprising a first charge region and a second charge region wherein a net charge in the first and second charge regions is reduced in a programming state for the nonvolatile memory.

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13. The system of claim 11 further comprising a tunnel layer over the channel.

14. The system of claim 13, the tunnel layer further comprising energy barriers for electrons and electric holes which are lower than those of the first isolating layer.

15. The system of claim 13, the tunnel layer further comprising at least one of titanium oxide and BST (barium, strontium and tantalum compound).

16. A method for operating a nonvolatile memory having at least one bit comprising:

erasing the at least one bit by retaining electrons in a trapping layer;

programming the at least one bit by injecting electric holes;

reading the at least one bit by applying a bias voltage;

detecting one of a threshold voltage and a read current for the at least one bit; and

providing one of a reference voltage and a reference current.

17. The method of claim 16 further comprising comparing the read current with the reference current wherein the at least one bit is erased if the read current is lower than the reference current.

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18. The method of claim 16 further comprising comparing the read current with the reference current wherein the at least one bit is programmed if the read current is larger than the reference current.

19. The method of claim 16 further comprising forming a tunnel layer over the channel.

20. The method of claim 19 further comprising forming the tunnel layer with at least one of titanium oxide and BST (barium, strontium and tantalum compound).

21. A method for operating a nonvolatile memory having a drain bit and a source bit comprising:

erasing one of the drain bit and the source bit by retaining electrons in a nitride layer in the nonvolatile memory;

programming the drain bit by injecting electric holes in a drain in the nonvolatile memory;

programming the source bit by injecting electric holes in a source in the nonvolatile memory; and

reading the drain bit and the source bit by applying a bias voltage to the source and the drain, respectively.

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22. The method of claim 21 wherein the drain bit is programmed by electron reduction in the drain bit.

23. The method of claim 21 wherein the source bit is programmed by electron reduction in the source bit.

24. The method of claim 21 further comprising providing one of a reference voltage and a reference current.

25. The method of claim 24 wherein one of the reference voltage and the reference current is provided in a sensing circuit having a driver and a comparator.

26. The method of claim 24 further comprising:

detecting a read current for the drain bit and the source bit, respectively; and

comparing the read current with the reference current for the drain bit and the source bit, respectively.

27. The method of claim 26 wherein the drain bit is erased if, at the drain, the read current is lower than the reference current.

28. The method of claim 26 wherein the source bit is erased if, at the source, the read current is lower than the reference current.

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29. The method of claim 26 wherein the drain bit is programmed if, at the drain, the read current is larger than the reference current.

30. The method of claim 26 wherein the source bit is programmed if, at the source, the read current is larger than the reference current.

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